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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/590,796	06/08/2000	Gordon J. Vreugdenhil	1467-14	9846

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 09/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/590,796	VREUGDENHIL ET AL.	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☒ Claim(s) *1* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Applicant's amendment to Claims 1-23 of U.S. Application 09/590,796 filed on 05/27/2004 is presented for examination. The amendment amends the specification, as well as claims 1, 2, 3, 9, and 12.
2. Applicant's arguments, see Amendment filed 5/27/2004, with respect to the rejection(s)of claim(s) 1-22 under 35 U.S.C. §112, §101, and double patenting, have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art, and applicant's admission in the above-cited amendment.
3. The newly found prior art, consisting of two articles by Christen, E. and Damon, D., "Introduction to VHDL-AMS: 1. Structural and Discrete Time Concepts", and "Introduction to VHDL-AMS: 2. Continuous and Mixed Continuous / Discrete Concepts" have publication dates of Sept. 15-18, 1996, and therefore pre-date the priority filing date the present application. These references address the dynamic scheduling of analog equations using VHDL-AMS. (The Sasaki reference, mentioned in the Conclusion section of the previous Office Action, post-dates the priority filing date).

Claim Interpretations

4. Applicants define the term "**slot**" in the Specification (p.4, lines 1-3) as follows (Emphasis added):

> "In a system of simultaneous equations, each system variable is said to have a "slot" and there is some set of equations that can be used to fill the slot in order to associate the system variable with an equation for solving the system of equations."

5. Examiner interprets the functionality of "simultaneous equations" as being equivalent to the "simultaneous statements" functionality taught in IEEE Standard 1076.1-1999. March 18, 1999. (See IEEE Std 1076.1-1999, pp.225, Section "15. Simultaneous Statements").

6. Applicants define the term "**analog solution iteration**" as follows (See Specification, p.4, lines 21-23):

> "An analog solution iteration is defined to occur when the analog solver requires that values need to be determined for the expressions forming the equations in the system."

7. Applicants define the term "**dynamic slot target variable**" as follows (See Specification, p.5, lines 7, and 11-14):

> "Assume that the partitioning results in a set of system variables Q_1 ... Q_m and ... For each *j* from 1 to *m*, generate a new unconditional association between the slot for [system variable] Q_j and a variable q'_j where q'_j is a new temporary variable that is otherwise undefined. Each q'_j is called the ***dynamic slot target*** variable for the associated [system variable] Q_j."

Claim Objections

8. Claim 1 is objected to because of the following informalities: The phrase "using the solution **tot eh** system ..." is grammatically incorrect. Appropriate correction is required.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The prior art used for these rejections is as follows:

11. Christen, E. et al., "Introduction to VHDL-AMS: 2. Continuous and Mixed Continuous / Discrete Concepts", Proc. of 1996 IEEE Int'l Symposium on Computer-Aided Control System Design. Sept. 15-18, 1996. (Henceforth referred to as "**Christen 2**").

12. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

13. **Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Christen 2 in view of Applicant's own admission.**

14. In regards to Claim 1, Christen 2 teaches the following limitations:

> Claim 1 (currently amended) In a computer simulation of a physical circuit or system including an analog or mixed signal digital-analog component, the physical circuit or

system described in a hardware description language and characterized by a system of simultaneous equations, the method comprising:

representing the physical circuit or system as a system of simultaneous equations, the system of simultaneous equations including a slot for an active conditional equation and a dynamic slot target variable associated with the slot in the system of simultaneous equations;
(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Example 6 on p.275)

Christen 2 teaches that "The *simultaneous case* and *if statements* allow the description of piecewise defined behavior. Each contains an arbitrary list of simultaneous statements in its statement parts, including nested simultaneous case and if statements. Only the simultaneous statements selected by the case expressions and chosen by the conditional expressions are considered by the analog solver."

Examiner interprets that the Applicant's claimed "slot for the active conditional equation" is inherently taught in Christen's teaching that "Only the simultaneous statements selected by the case expressions and chosen by the conditional expressions are considered by the analog solver," because without a "slot" for the active conditional equation, Christen's teaching would not work.

Moreover, Examiner interprets that Applicant's claimed "dynamic slot target variable associated with the slot in the system of simultaneous equations" is also taught in Christen. In Christen's Example 6 (on p.275), "v'dot" is a dynamic slot target variable associated with the slot in the system of simultaneous equations.

selecting an active conditional equation at a current analog solution iteration;
(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Example 6 on p.275)

Christen 2 makes reference to an "analog solver" in p.271, col.2, para.1, and also in p.270, col.2, para.4: "Only the results that the analog solver must achieve, and not its algorithm, are characterized in the language definition."

assigning a value for the active conditional equation to a dynamic slot target variable at the current analog solution iteration, thereby associating the active conditional equation with a slot in the system of simultaneous equations;
(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Example 6 on p.275)

However, Christen 2 does not expressly teach the following limitations:

solving the system of simultaneous equations; and

using the solution tot eh system of simultaneous equations to validate the physical circuit or system;

wherein said representing said selecting, said assigning, said solving and said using are performed in a computer system.

In regards to the "using the solution to the system of simultaneous equations to validate the physical circuit or system", Examiner finds this limitation to be merely an intended use of the invention.

In regards to "solving the system of simultaneous equations", Christen 2 teaches (p.270, col.2, para.4) that "The VHDL 1076.1 language therefore must provide a notation for DAEs, but the language definition can remain neutral with regard to the selection of numerical methods. The definition of the language specifies what system of equations (at each time) is described by the text of a model. The solution itself is referred to as the 'analog solver.' Only the results that the analog solver must achieve, and not its algorithm, are characterized in the language definition."

However, by Applicant's own admission (see amendment dated 5/27/2004, p.13, paragraph 3), the Applicant argues that:

> Applicants submit that the Examiner must take into account the level of skill in the art, including knowledge of many well known methodologists to solve sets of simultaneous equations. For example, the skilled artisan is presumed to be knowledgeable of methods described in basic text books, suchas G. Dahlquist, A. Bjork: 'Numerical Methods', Prentice-Hall, 1974 and R.W. Hamming: 'Numerical Methods for Scientists and Engineers', McGraw-Hill, 1962. ... In view of the above, Applicants submit that any skilled artisan would immediately understandstand that any prior art method (**even Newton's method**) can be used to solve a set of simultaneous equations of the type prepared by the methodology being claimed.

Examiner therefore finds that the "solving the system of simultaneous equations", and performing this solving in a computer system, is admitted prior art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Christen with numerical methods such as Newton's method, or the numerical methods described in basic text books, such as G. Dahlquist, A. Bjork: 'Numerical Methods', and R.W. Hamming: 'Numerical Methods for Scientists and

Engineers', because this is Applicant's admission in the amendment dated 5/27/2004 (see p.13, paragraph 3).

15. In regards to Claim 2, Christen 2 teaches the following limitations:

Claim 2 (currently amended) A method of solving a system of simultaneous equations including one or more conditional equations, the system of simultaneous equations describing a physical circuit or system in a hardware description language, the circuit including an analog component, the method comprising:

representing the physical circuit or system as a system of simultaneous equations, the system of simultaneous equations including one or more slots for an active conditional equation and a dynamic slot target variable associated with the slot for active conditional equations selected from a set of possible characteristic expressions and one or more dynamic slot target variables associated with the slots in the system of simultaneous equations;
(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Example 6 on p.275)

Christen 2 teaches that "The *simultaneous case* and *if statements* allow the description of piecewise defined behavior. Each contains an arbitrary list of simultaneous statements in its statement parts, including nested simultaneous case and if statements. Only the simultaneous statements selected by the case expressions and chosen by the conditional expressions are considered by the analog solver."

Examiner interprets that the Applicant's claimed "slot for the active conditional equation" is inherently taught in Christen's teaching that "Only the simultaneous statements selected by the case expressions and chosen by the conditional expressions are considered by the analog solver," because without a "slot" for the active conditional equation, Christen's teaching would not work.

Moreover, Examiner interprets that Applicant's claimed "dynamic slot target variable associated with the slot in the system of simultaneous equations" is also taught in Christen. In Christen's Example 6 (on p.275), "v'dot" is a dynamic slot target variable associated with the slot in the system of simultaneous equations.

selecting a set of active conditional equations at a current analog solution iteration;
(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Example 6 on p.275)

Christen 2 makes reference to an "analog solver" in p.271, col.2, para.1, and also in p.270, col.2, para.4: "Only the results that the analog solver must achieve, and not its algorithm, are characterized in the language definition."

assigning a value for each active conditional equation in the set of active conditional equations to a dynamic slot target variable at the current analog solution iteration, thereby associating the active conditional equation with a slot in the system of simultaneous equations; and
(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Example 6 on p.275)

However, Christen 2 does not expressly teach the following limitations:

solving the system of simultaneous equations at the current analog solution iteration;

wherein said representing, said selecting, said assigning, and said solving are performed in a computer system.

In regards to "solving the system of simultaneous equations", Christen 2 teaches (p.270, col.2, para.4) that "The VHDL 1076.1 language therefore must provide a notation for DAEs, but the language definition can remain neutral with regard to the selection of numerical methods. The definition of the language specifies what system of equations (at each time) is described by the text of a model. The solution itself is referred to as the 'analog solver.' Only the results that the analog solver must achieve, and not its algorithm, are characterized in the language definition."

However, by Applicant's own admission (see amendment dated 5/27/2004, p.13, paragraph 3), the Applicant argues that:

> Applicants submit that the Examiner must take into account the level of skill in the art, including knowledge of many well known methodologists to solve sets of simultaneous equations. For example, the skilled artisan is presumed to be knowledgeable of methods described in basic text books, suchas G. Dahlquist, A. Bjork: 'Numerical Methods', Prentice-Hall, 1974 and R.W. Hamming: 'Numerical Methods for Scientists and Engineers', McGraw-Hill, 1962. ... In view of the above, Applicants submit that any skilled artisan would immediately understandstand that any prior art method (**even Newton's method**) can be used to solve a set of simultaneous equations of the type prepared by the methodology being claimed.

Examiner therefore finds that the "solving the system of simultaneous equations", and performing this solving in a computer system, is admitted prior art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Christen with the methods described in basic text books, such as G. Dahlquist, A. Bjork: 'Numerical Methods', and R.W. Hamming: 'Numerical Methods for Scientists and Engineers', because this is Applicant's admission in the amendment dated 5/27/2004 (see p.13, paragraph 3).

16. In regards to Claim 3, Christen 2 teaches the following limitations:

Claim 3 (currently amended) A method according to claim 2, the method further comprising:

said computer selecting a **second set** of active conditional equations at a second current analog solution iteration;

(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Examples 5 and 6 on p.275)

said computer assigning a value for each active conditional equation in the second set of active conditional equations to a dynamic slot target variable at the **second current analog solution iteration**, thereby associating the active conditional equation with a slot in the system of simultaneous equations; and

(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Examples 5 and 6 on p.275)

However, Christen 2 does not expressly teach the following limitations:

said computer solving the system of simultaneous equations at the second current analog solution iteration.

In regards to "solving the system of simultaneous equations", Christen 2 teaches (p.270, col.2, para.4) that "The VHDL 1076.1 language therefore must provide a notation for DAEs, but the language definition can remain neutral with regard to the selection of numerical methods. The definition of the language specifies what system of equations (at each time) is described by the text of a model. The solution itself is referred to as the 'analog solver.' Only the results that the analog solver must achieve, and not its algorithm, are characterized in the language definition."

However, by Applicant's own admission (see amendment dated 5/27/2004, p.13, paragraph 3), the Applicant argues that:

> Applicants submit that the Examiner must take into account the level of skill in the art, including knowledge of many well known methodologists to solve sets of simultaneous equations. For example, the skilled artisan is presumed to be knowledgeable of methods described in basic text books, suchas G. Dahlquist, A.

> Bjork: 'Numerical Methods', Prentice-Hall, 1974 and R.W. Hamming: 'Numerical Methods for Scientists and Engineers', McGraw-Hill, 1962. ... In view of the above, Applicants submit that any skilled artisan would immediately understandstand that any prior art method (**even Newton's method**) can be used to solve a set of simultaneous equations of the type prepared by the methodology being claimed.

Examiner therefore finds that the "solving the system of simultaneous equations", and performing this solving in a computer system, is admitted prior art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Christen with the methods described in basic text books, such as G. Dahlquist, A. Bjork: 'Numerical Methods', and R.W. Hamming: 'Numerical Methods for Scientists and Engineers', because this is Applicant's admission in the amendment dated 5/27/2004 (see p.13, paragraph 3).

17. In regards to Claim 4, Christen 2 teaches the following limitations:

Claim 4 (original) A method according to claim 2, wherein assigning a value for each active conditional equation includes relating a system variable to each active conditional equation for the current analog solution iteration.

(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Examples 5 and 6 on p.275)

18. In regards to Claim 5, Christen 2 does not expressly teach the following:

Claim 5 (original) A method according to claim 4, wherein solving the system of simultaneous equations includes determining a value for each system variable related to an active conditional equation.

In regards to "solving the system of simultaneous equations", Christen 2 teaches (p.270, col.2, para.4) that "The VHDL 1076.1 language therefore must provide a notation for DAEs, but the language definition can remain neutral with regard to the selection of numerical methods. The definition of the language specifies what system of equations (at each time) is described by the text of a model. The solution itself is referred to as the 'analog solver.' Only the results that the analog solver must achieve, and not its algorithm, are characterized in the language definition."

However, by Applicant's own admission (see amendment dated 5/27/2004, p.13, paragraph 3), the Applicant argues that:

> Applicants submit that the Examiner must take into account the level of skill in the art, including knowledge of many well known methodologists to solve sets of simultaneous equations. For example, the skilled artisan is presumed to be knowledgeable of methods described in basic text books, suchas G. Dahlquist, A. Bjork: 'Numerical Methods', Prentice-Hall, 1974 and R.W. Hamming: 'Numerical Methods for Scientists and Engineers', McGraw-Hill, 1962. ... In view of the above, Applicants submit that any skilled artisan would immediately understandstand that any prior art method (**even Newton's method**) can be used to solve a set of simultaneous equations of the type prepared by the methodology being claimed.

Examiner therefore finds that the "solving the system of simultaneous equations", and performing this solving in a computer system, is admitted prior art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Christen with the methods described in basic text books, such as G. Dahlquist, A. Bjork: 'Numerical Methods', and R.W. Hamming: 'Numerical Methods for Scientists and Engineers', because this is Applicant's admission in the amendment dated 5/27/2004 (see p.13, paragraph 3).

19. In regards to Claim 6, Christen 2 teaches the following limitations:

Claim 6 (original) A method according to claim 2, wherein at most one conditional equation is assigned to each dynamic slot target variable at the current analog solution iteration.

(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Examples 5 and 6 on p.275)

20. In regards to Claim 7, Christen 2 teaches the following limitations:

Claim 7 (original) A method according to claim 2, wherein each conditional equation is assigned to at most one dynamic slot target variable at the current analog solution iteration.

(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Examples 5 and 6 on p.275)

21. In regards to Claim 8, Christen 2 teaches the following limitations:

Claim 8 (original) A method according to claim 2, wherein the number of active conditional equations is required to be equal to the number of dynamic slot target variables.

(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Examples 5 and 6 on p.275)

22. In regards to Claim 9, Christen 2 teaches the following limitations:

Claim 9 (currently amended) A method according to claim 8, the method further comprising said computer reporting a simulation failure if the number of active conditional equations differs from the number of dynamic slot target variables while attempting to solve the system of simultaneous equations.

(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Examples 5 and 6 on p.275)

23. In regards to Claim 10, Christen 2 teaches the following limitations:

Claim 10 (original) A method according to claim 2, wherein selecting an active conditional equation includes evaluating a condition associated with the active conditional equation.

(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Examples 5 and 6 on p.275)

24. In regards to Claim 11, Christen 2 teaches the following limitations:

Claim 11 (original) A method according to claim 10, wherein evaluating a condition occurs before selecting the active conditional equation.

(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Examples 5 and 6 on p.275)

25. Claims 12-21 are rejected based on the same reasoning as claims 2-11. Claims 12-21 are computer-readable medium containing a program claims reciting the equivalent limitations as are recited in method claims 2-11 and taught throughout Christen 2 and Applicant's Own Admission.

26. In regards to Claim 22, Christen 2 teaches the following limitations:

Claim 22 (original) An apparatus for simulating a circuit, solving a system of simultaneous equations including a conditional equation, the system of simultaneous equations describing a physical circuit or system in a hardware description language, the circuit including an analog component, the apparatus comprising:

a computer for simulating the physical circuit or system;
(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Example 6 on p.275)

a hardware description language description of the physical circuit or system stored on a computer-readable medium;
(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Example 6 on p.275)

means for selecting a set of active conditional equations;

(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Example 6 on p.275)

means for assigning a value for each active conditional equation in the set of active conditional equations to a dynamic slot target variable at the current analog solution iteration, thereby associating the active conditional equation with a slot in the system of simultaneous equations; and
(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Example 6 on p.275)

Christen 2 teaches that "The *simultaneous case* and *if statements* allow the description of piecewise defined behavior. Each contains an arbitrary list of simultaneous statements in its statement parts, including nested simultaneous case and if statements. Only the simultaneous statements selected by the case expressions and chosen by the conditional expressions are considered by the analog solver."

Examiner interprets that the Applicant's claimed "slot for the active conditional equation" is inherently taught in Christen's teaching that "Only the simultaneous statements selected by the case expressions and chosen by the conditional expressions are considered by the analog solver," because without a "slot" for the active conditional equation, Christen's teaching would not work.

Moreover, Examiner interprets that Applicant's claimed "dynamic slot target variable associated with the slot in the system of simultaneous equations" is also taught in Christen. In Christen's Example 6 (on p.275), "v'dot" is a dynamic slot target variable associated with the slot in the system of simultaneous equations.

However, Christen 2 does not expressly teach the following limitations:

translation software to translate the hardware description language description into a system of simultaneous equations, the system of simultaneous equations including one or more slots for conditional equations selected from a set of possible conditional equations;

means for solving the system of simultaneous equations at the current analog solution.

In regards to the translation software, by Applicant's own admission (see amendment dated 5/27/2004, p.13, paragraph 3), the Applicant argues that:

> The apparatus is being claimed in Claims 22 and 23 at a generic level, regardless of any internal form to which HDL code may be translated. As is well known in the art, there are many conventional

> methods which identify how HDL code is to be represented internally, depending on the implementation.
>
> In fact, even the Examiner acknowledged that there are many conventional methods by stating "[g]iven the large number of possible solutions ..." (in the middle of page 6 of the Office Action). Hence, any single one of the "large number of possible solutions" acknowledged by the Examiner may be used to realize the benefits of the claimed invention. Therefore, Applicants submit that **no** experimentation is required to use an otherwise normally working apparatus, for solving simultaneous equations after being prepared as claimed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Christen with "any single one" of the "large number of [well known] possible solutions" for translating HDL code, because this is Applicant's admission in the amendment dated 5/27/2004 (see p.14, paragraphs 3-4).

In regards to "solving the system of simultaneous equations", Christen 2 teaches (p.270, col.2, para.4) that "The VHDL 1076.1 language therefore must provide a notation for DAEs, but the language definition can remain neutral with regard to the selection of numerical methods. The definition of the language specifies what system of equations (at each time) is described by the text of a model. The solution itself is referred to as the 'analog solver.' Only the results that the analog solver must achieve, and not its algorithm, are characterized in the language definition."

However, by Applicant's own admission (see amendment dated 5/27/2004, p.13, paragraph 3), the Applicant argues that:

> Applicants submit that the Examiner must take into account the level of skill in the art, including knowledge of many well known methodologists to solve sets of simultaneous equations. For example, the skilled artisan is presumed to be knowledgeable of methods described in basic text books, suchas G. Dahlquist, A. Bjork: 'Numerical Methods', Prentice-Hall, 1974 and R.W. Hamming: 'Numerical Methods for Scientists and Engineers', McGraw-Hill, 1962. ... In view of the above, Applicants submit that any skilled artisan would immediately understandstand that any prior art method (**even Newton's method**) can be used to solve a set of simultaneous equations of the type prepared by the methodology being claimed.

Examiner therefore finds that the "solving the system of simultaneous equations", and performing this solving in a computer system, is admitted prior art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Christen with the methods described in basic text books, such as G. Dahlquist, A. Bjork: 'Numerical Methods', and R.W. Hamming: 'Numerical Methods for Scientists and Engineers', because this is Applicant's admission in the amendment dated 5/27/2004 (see p.13, paragraph 3).

27. In regards to Claim 23, Christen 2 teaches the following limitations:

Claim 23 (original) An apparatus according to claim 22, wherein the means for selecting an active conditional equation includes means for testing a condition associated with the active conditional equation.
(Christen 2, especially: p.271, col.2, para.1 - "*simultaneous case* and *if statements*"; and Example 6 on p.275)

Response to Arguments

Re: Claim Interpretations

28. Applicants persuasively argue (p.10 of the amendment filed 5/27/04) that the Examiner should change the Claim interpretation for the term "slot" in view of the proposed amendment to the specification. Therefore, the claim interpretation for the term "slot" has been changed.

29. Applicants unpersuasively argue (p.10 of the amendment filed 5/27/04) that the Examiner's interpretation of "simultaneous equations" being equivalent to "simultaneous statements" is incorrect because simultaneous statements only define a subset of all equations as per IEEE (section 12.1, 1st paragraph; and section 12.6.5, 2nd paragraph). Examiner has reviewed the cited paragraphs and does not find support for

Applicant's argument. Applicant is requested to provide a further explanation for citing these paragraphs.

30. Examiner acknowledges and agrees with Applicants' discussion of the terms "characteristic expression" and "conditional equation" in pp.10-11 of the amendment filed 5/27/04.

31. Examiner acknowledges the Applicants' amendment to Claims 1 and 12, and has withdrawn the objections from the previous Office Action.

Re: Specification Objections

32. The amendment filed 5/27/2004 overcomes the objection pertaining to page 3 of the specification has blank lines associated with the U.S. Patent Application Serial Number and the filing date of a specific application. The objection has been withdrawn.

33. The amendment to phrase beginning at page 2, line 10 of the specification is supported elsewhere in the Specification (p.4, lines 1-3). Therefore, the amendment to the specification has been entered.

Re: Double Patenting Rejection

34. Examiner has found Applicants' arguments regarding the double patenting rejections in the amendment filed 5/27/2004 to be persuasive, and is withdrawing the double patenting rejections.

Re: Claim Rejections - 35 USC § 112

35. Applicants persuasively argue (amendment filed 5/27/2004, p.13) that, based on the IEEE reference, one of ordinary skill in the art would know that the base type of the simultaneous equations is floating point and not integer. Examiner notes that this was not taught in the specification.

36. Examiner respectfully disagrees with Applicants' arguments (amendment filed 5/27/2004, p.15) that the rejection based on missing elements is based on 35 U.S.C. §112, first paragraph, and not the second paragraph (as cited in the previous Office Action). Examiner refers the Applicants to Form Paragraphs 7.34.12 and 7.34.13 in the MPEP.

37. However, Examiner has found the substance of Applicants' arguments regarding the 35 USC § 112 rejections in the amendment filed 5/27/2004 to be persuasive, and is withdrawing the 35 USC § 112 rejections.

Re: Claim Rejections - 35 USC § 101

38. Examiner has found Applicants' arguments regarding the 35 U.S.C. §101 rejections in the amendment filed 5/27/2004 to be persuasive, and is withdrawing the 35 U.S.C. §101 rejections.

Conclusion

39. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure.

40. Christen, E. et al., "Introduction to VHDL-AMS: 1. Structural and Discrete Time Concepts", Proc. of 1996 IEEE Int'l Symposium on Computer-Aided Control System Design. Sept. 15-18, 1996. (Henceforth referred to as "**Christen 1**"). This is the introductory article. The cited reference used in the claim rejection, Christen 2, is a continuation of this article.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone numbers are (703) 306-0297 and (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
2121 Crystal Drive
Arlington, VA

Fax: (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is:

(703) 305-3900.

Ayal I. Sharon

Art Unit 2123

August 31, 2004

JEAN R. HOMERE
PRIMARY EXAMINER